

CLAIMS

1. A semiconductor device comprising:
a top region of a second conductivity type;
5 a deep region of the second conductivity type;
an intermediate region of a first conductivity type for isolating the top region and the deep region; and
a trench gate facing a portion of the intermediate region via an insulating layer, wherein the portion facing the trench gate isolates the top region and the deep
10 region, and wherein the trench gate extends along a longitudinal direction and width of the trench gate varies along the longitudinal direction.

2. A semiconductor device according to claim 1,
wherein a plurality of trench gates extending in parallel is provided, and
15 variations of width of each trench gate along the longitudinal direction are aligned in phase.

3. A semiconductor device according to claim 1 or 2,
wherein a pair comprising a wide trench gate and a narrow trench gate is
20 repeated along the longitudinal direction, and total length of the wide trench gates is 30 to 80 % of the total length of the trench gate.

4. A semiconductor device according to any of the preceding claims,
wherein variations of width of each trench gate along the longitudinal direction are
25 repeated cyclically along the longitudinal direction.

5. A semiconductor device according to any of the preceding claims,
wherein width of the intermediate region interposed between adjacent wide trench gates is narrow such that the interposed region becomes a depressed region when
30 on-voltage is not being applied to the trench gates.

6. A semiconductor device according to any of the preceding claims,
wherein the top region is an emitter of IGBT and the deep region is a drift
of IGBT.

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7. A semiconductor device according to any of the preceding claims,
wherein the top region is a source of MOS and the deep region is a drift of
MOSFET.